CommAgility Limited
Charnwood Building,
Holywell Park, Loughborough,
Leicestershire LE11 3AQ, UK.
Tel +44 (0) 1509 228866
www.commagility.com

CommAgility AMC-RF2x2 Uses Xilinx® Virtex®-6 to Support LTE 2x2 MIMO

Paul A. Moakes
Technical Director, CommAgility Limited

Introduction

As 3GPP Long Term Evolution (LTE) technology moves into deployment, the requirement for LTE radio frequency (RF) air interface development and testing has driven demand for high bandwidth multi-banded multi-protocol universal radio interface cards.

CommAgility has long been recognised as a supplier of baseband LTE hardware solutions. Our latest products based on the Xilinx Virtex-6, such as the AMC-2C6670, have been adopted by customers around the world for LTE applications. It was therefore not surprising that we were approached by those customers with a requirement to also supply their RF interface as well as a processing module, to provide a complete one-stop shop for their LTE solution.

Our experience with the Xilinx Virtex-6 in baseband designs enabled us to rapidly develop a highly flexible 2x2 multiple-input multiple-output (MIMO) LTE RF interface module, the AMC-RF2x2. This card, now a commercially available product from CommAgility, covers all LTE bands, bandwidths, and duplex types. Xilinx's flexible IO interfaces and comprehensive range of wireless IP cores meant that we could rapidly develop the solution from concept to delivery in under six months.

The scalability and flexibility of the Virtex-6 range makes possible a straightforward roadmap transition to LTE-Advanced and 4x4 MIMO support. Beyond this, the introduction of Xilinx's next generation Kintex-7 devices will bring performance enhancement and power reduction, with the possibility to bring some of the baseband processing onto the RF card.

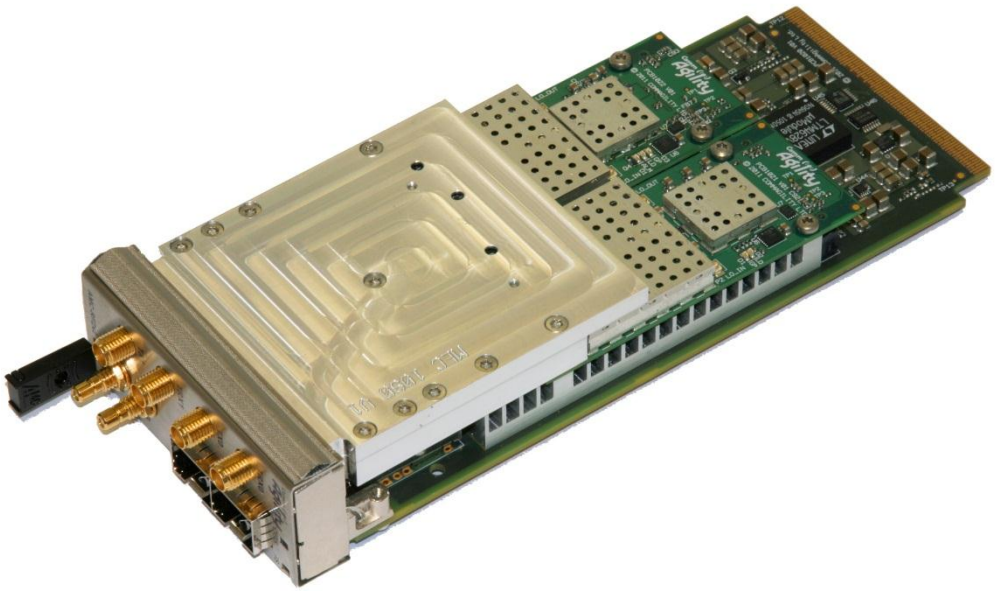

Figure 1. AMC-RF2x2

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The AMC-RF2x2 (www.commagility.com/amc-rf2x2.php) is a full-size single-width Advanced Mezzanine Card (AMC) as defined by PICMG (www.picmg.org) It is designed for use in a Micro Telecommunications Computing Architecture (MicroTCA) chassis alongside other AMCs, allowing a system solution to be created which is configurable at the card level.

For example, a three-sector base station system may require three AMC-RF2x2 cards, one for each sector. However, a single CommAgility AMC-2C6670 (www.commagility.com/amc-2c6670.php), is able to provide LTE baseband processing for all three sectors. A MicroTCA chassis could thus be populated with one AMC-2C6670 and three AMC-RF2x2 cards, with a processor AMC (PrAMC) to provide media access and management functionality. Such a system is shown in Figure 2.

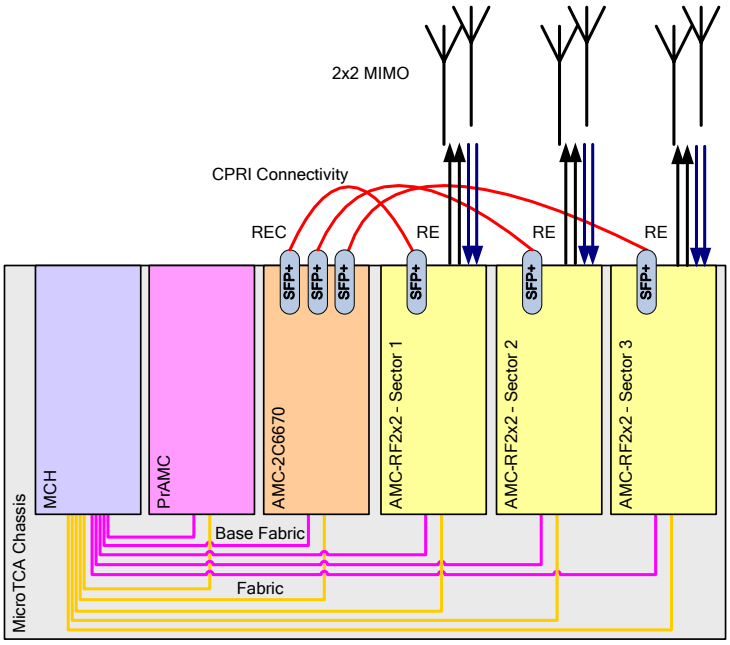

Figure 2. Three Sector Base Station Architecture

The MicroTCA backplane allows communication between the AMCs using the Ethernet base fabric for control and the fabric (Serial Rapid IO (SRIO), Ethernet 10 Gigabit Unit Attachment Interface (XAUI), or PCI Express (PCIe)) for data. The MicroTCA Controller Hub (MCH) provides the switching fabric for the MicroTCA chassis, and also supports reliability and availability features such as hot card swapping and card temperature monitoring.

Baseband Data Path and Clock Synchronisation

In the system shown in Figure 2, communication between the AMC-2C6670 and AMC-RF2x2 cards is over a Common Public Radio Interface (CPRI) link (www.cpri.info). This link runs at 4.9152Gbaud and can use either an optical or copper physical interface based on the SFP+ modules used on the cards. The CPRI link carries two channels of IQ data to and from the RF card to support MIMO operation. It is able to support LTE channel bandwidths of 1.4MHz, 3MHz, 5MHz, 10MHz, 15MHz, 20MHz and 40MHz.

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The FPGA CPRI interface is implemented using the Xilinx CPRI IP core (http://www.xilinx.com/products/intellectual-property/DO-DI-CPRI.htm) and is able to support line rates up to 9.8 Gbaud for Xilinx 7-Series and up to 6.144 Gbaud for Virtex-6 platform. The AMC-2C6670 acts as the CPRI radio equipment controller (REC) and generates the master clock for the CPRI link. This is derived from a GPS receiver on the card, ensuring clock synchronisation between equipment linked across the air interface.

This reference clock is extracted by the Virtex-6 MGT block, acting as the radio equipment (RE), and passed to a phase-locked loop (PLL) for jitter cleaning. The cleaned clock is then used for the air interface timing as shown in Figure 3.

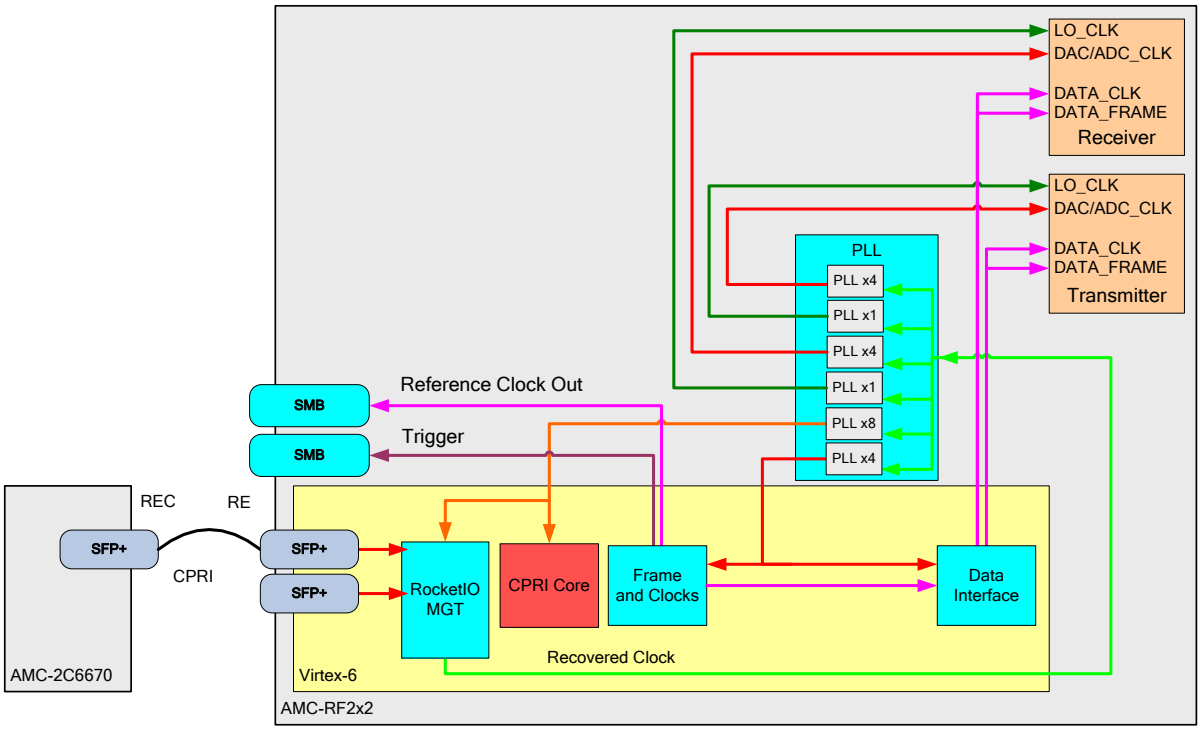

Figure 3. AMC-RF2x2 Clock Synchronisation

The AMC-RF2x2 can also support IQ data transfer and control over the MicroTCA fabric using PCIe, XAUI or SRIO protocols with transfer rates up to 20Gbps. The fabric selection can be made automatic using AMC e-keying and the flexible configuration of the Virtex-6 MGT ports to support the protocol choice. This allows the card to be more closely integrated into a chassis based system where IQ data is distributed across multiple cards.

Radio Interface

On arrival at the FPGA the IQ samples are de-interleaved from the CPRI frame according to the 3GPP E-UTRA specification (www.3gpp.org) using custom logic then passed on to the Virtex-6 digital up converters (DUCs) as shown in Figure 4.

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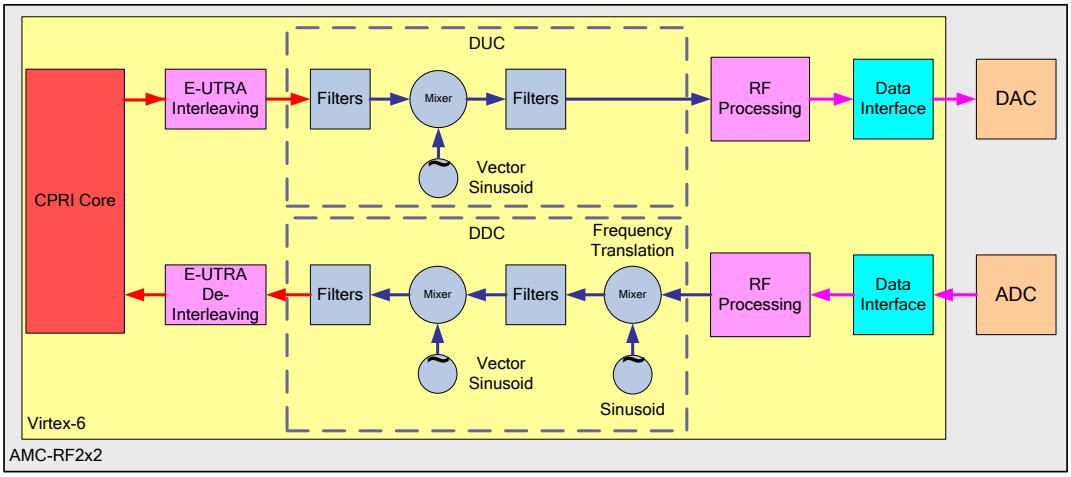

Figure 4. AMC-RF2x2 Clock Synchronisation

The AMC-RF2x2 uses the Xilinx LogiCORE™ DUC/DDC Compiler (http://www.xilinx.com/products/intellectual-property/DUC_DDC_Compiler.htm) for this operation. This allowed the DUC and DDC design to be implemented and simulated ahead of the interface components being available. The core directly supports the 5MHz, 10MHz, and 20MHz LTE bandwidth sample rates of 7.68Msps, 15.36Msps, and 30.72Msps used on the AMC-RF2x2. The Xilinx LogiCore finite impulse response (FIR) Filter Compiler (http://www.xilinx.com/products/intellectual-property/FIR_Compiler.htm) has been used to develop support for 1.4MHz, 3MHz, and 15MHz bandwidths using these same sample rates. The use of Xilinx DSP slices allows the DAC/DUC to be efficiently implemented using a minimum of FPGA resources.

The DUC filters the baseband data and converts it to the higher sample rate of 61.44MHz required by the RF digital-to-analogue converter (DAC). In the AMC-RF2x2, the DAC itself can then perform a further up-conversion to the required sample rate of 983.04MHz. Additional IP cores can be added to support crest factor reduction and digital pre-distortion which are required for broadcast transmission. However, in the wireless test application under discussion, these features are also left unused.

The RF processing block following the DUC implements gain control. IQ imbalance and DC offset correction are supported in the DAC, and the Virtex-6 acts as a control interface for this DAC functionality. IQ imbalance and DC offset correction are performed automatically in the AMC-RF2x2 whenever the operating mode or operating band of the AMC-RF2x2 is changed.

With the IQ data at the correct rate, it is now passed to the DACs for processing in the analogue domain. On the AMC-RF2x2, the DACs and analogue-to-digital converters (ADCs) use a DDR interface implemented using LVDS signals from the FPGA SelectIO. The clocking blocks within the FPGA allow the interfaces to be synchronised to the main card clocks.

In the receive path, data from the ADCs is sent to an RF processing block. This implements the gain control, IQ imbalance and DC offset correction automatically before data is down-mixed from Low-IF to baseband and then passed to the digital down converter (DDC). The DDC filters digital signal from the ADC and reduces the sample rate from 122.88MHz to the CPRI rate for the receive bandwidth, e.g. 30.72MHz for 20MHz bandwidth. Finally, the IQ samples pass through a gain control block before being interleaved into a CPRI frame according to the E-UTRA specification.

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Control and Management

The various on-card devices in the RF chain are managed by a mixture of serial peripheral interface (SPI) busses and general purpose IO (GPIO). The implementation of these busses is subtly different for each device and requires careful inspection of the data sheet timing diagrams. Using the Virtex-6 to support these interfaces allows these variations to be accommodated, while presenting a common control interface.

On-card memory is provided in the form of 128Mbytes of non-volatile Flash memory and 128Mbytes of volatile DDR3 SDRAM. Using the memory interface generator (MIG), it is straight forward to implement support for external DDR3 from the Virtex-6.

Logic in the Virtex-6 is used to present a unified interface to these multiple control busses and to aggregate common functions associated with particular modes of operation. The supported modes of the AMC-RF2x2 are shown in Table 1.

Mode	Description
Loopback	Transmit signal is connected to the receive path by-passing the channel combination stages.
TDD	Common transmit and receive interfaces. Signals are combined using a time division duplex switch.
Combined	Common transmit and receive interfaces. Signals combined using a resistive network.
Wideband	Separate transmit and receive interfaces.

Table 1. AMC-RF2x2 Supported Operational Modes

This unified interface is presented to the card support software for control. This software runs on a MicroBlaze soft processor core on the Virtex-6, which connects to peripherals using the Advanced eXtensible Interface 4 (AXI-4) protocol. AXI-4 makes peripheral integration easier by offering a standard interface for all devices.

Capture and play-out of IQ data is supported using internal Block-RAM based storage. Larger buffers are stored by using the Block-RAM to cache data for periodic transfer to the external SDRAM.

A lightweight IP stack is implemented for the MicroBlaze, which allows a telnet session to establish a link with the card. This provides an interface for simple remote control of the card over Ethernet on the AMC base fabric.

To support AMC-RF2x2 based developments, CommAgility provides a PC-based graphical user interface-(GUI)-based front end for the telnet control. Implemented using National Instruments LabVIEW, the simple telnet interface is used to provide a rich control environment. The GUI is shown in Figure 5.

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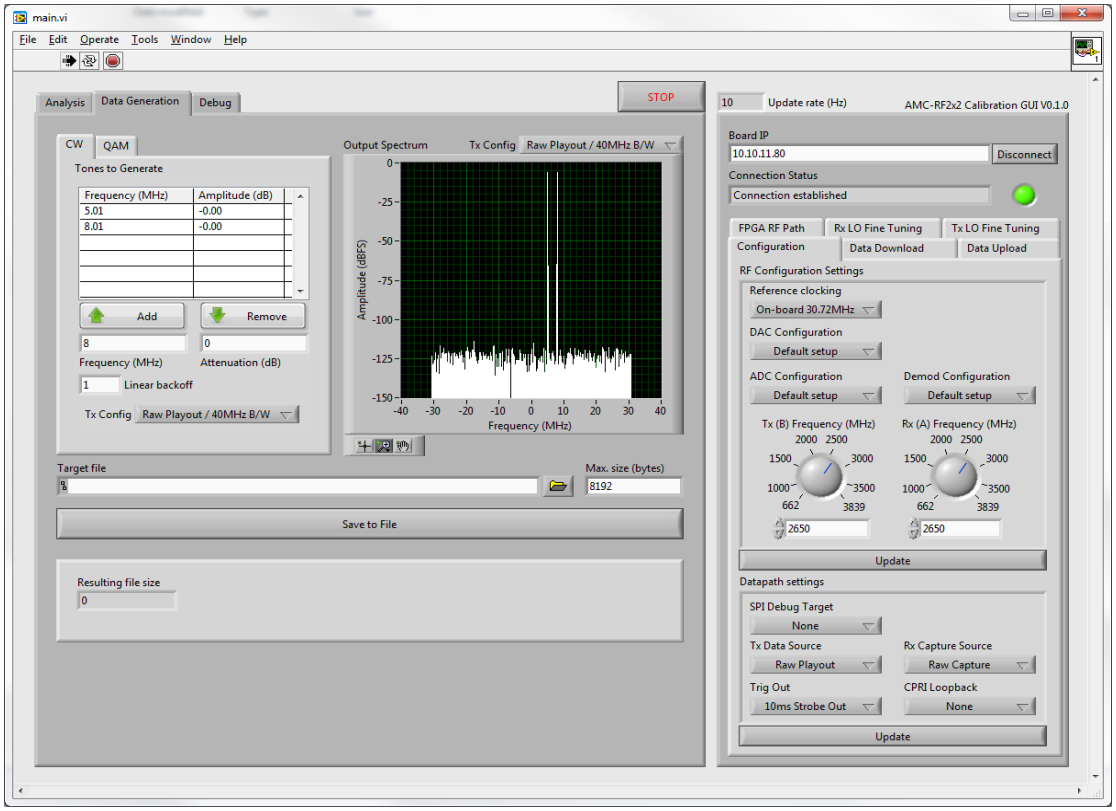

Figure 5. AMC-RF2x2 Control GUI

The CPRI link also includes the Fast Control and Maintenance (Fast C&M) channel. The CPRI IP core Fast C&M interface connects to a Xilinx MII interface supporting an Ethernet interface at speeds of over 100Mbps. This allows the Fast C&M channel to support the telnet interface described above. Using the Fast C&M channel, the AMC-2C6670 can control the AMC-RF2x2, for example to read the on-card temperature sensors and support temperature compensation.

Conclusion

The Xilinx Virtex-6 has a perfect mix of physical interfaces for implementing a wireless front end AdvancedMC card. The device chosen by CommAgility is the LX75T, which is more than adequate for the application described in this white paper. For more demanding performance, the FPGA footprint supports a family of devices right up to the powerful LX240T.

Furthermore, with the establishment of the AMC-RF2x2 for 2x2 MIMO in CommAgility's portfolio, the scalability and flexibility of the Virtex-6 range makes possible a straightforward roadmap transition to LTE-Advanced and 4x4 MIMO support. Beyond this, the introduction of Xilinx's next generation Kintex-7 devices enables power reduction and the possibility to bring some of the baseband processing onto the RF card.

However, the underlying device is only a part of the jigsaw. The provision of Xilinx LogiCORE IP for the full range of building blocks required in the wireless signal chain has accelerated development. Using Xilinx cores with proven operation and optimal resource usage has greatly reduced CommAgility's development and test time, bringing the card to market in less than six months.