

AMC-V5Fe

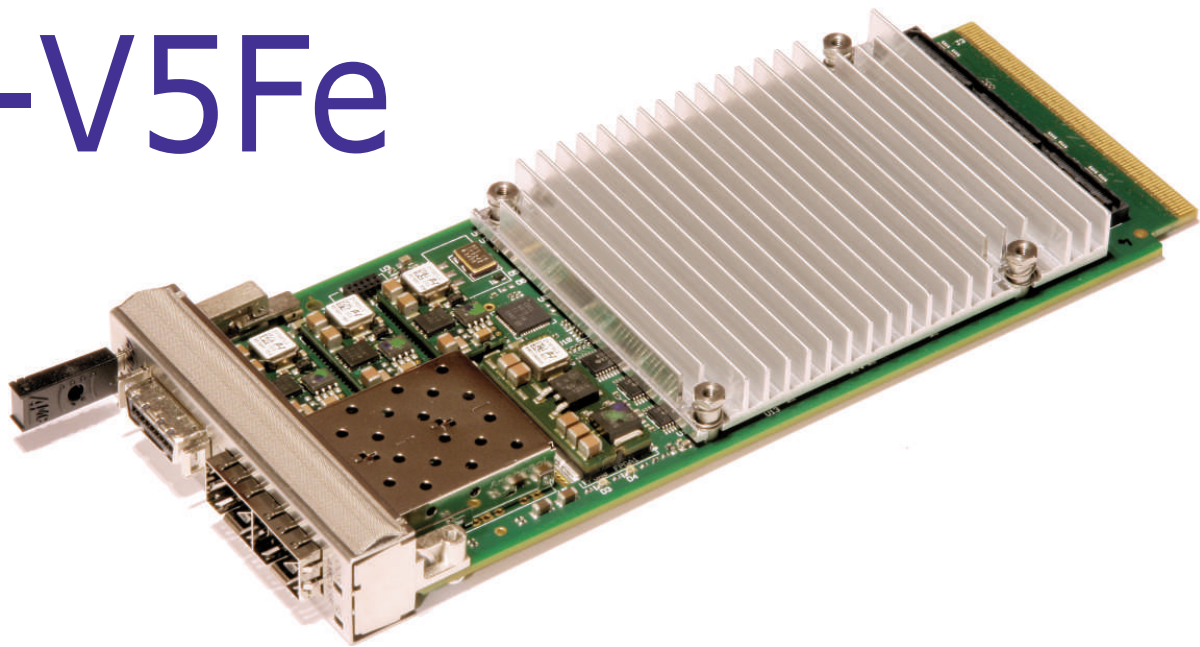
DATASHEET

A high performance FPGA based interface and processing card for a range of I/O and processing applications

4x PCI Express and dual Gigabit Ethernet connections to Host CPU via AMC ports on edge connector

Dual Optical SFP and 4x serial front panel interfaces supporting a range of serial I/O standards; flexible clock synchronisation

Mezzanine site with front panel access allows custom I/O or processing capability to be added



KEY FEATURES

- ◆ Xilinx Virtex-5 LX110T FPGA, customer programmable (alternatives also possible)
- ◆ 4x direct PCI Express connection from FPGA to AMC ports 4-7
- ◆ Dual highly flexible optical front panel interfaces, for wireless antenna or other high speed data links
- ◆ Front panel CX4 connector for 10 Gbps serial data links
- ◆ Advanced clock recovery and synchronisation options including master and slave modes; AMC, front panel and GPS clocks
- ◆ Full Gigabit Ethernet infrastructure
- ◆ Single width, mid or full-size PICMG AMC.0 R2.0 Advanced Mezzanine Card
- ◆ Software and firmware library support
- ◆ Developed for use in OEM products

RESULTING BENEFITS

- + High performance FPGA resource
- + Low latency, high performance connection to MicroTCA Host or other CPU
- + Industry standard CPRI and OBSAI links to wireless radios, base stations under test, or other optical data links such as SRIO
- + High performance connection to I/O or other system elements
- + Covers multiple requirements for Base Stations and Test Equipment; GPS clock sync avoids a separate card in the system
- + Industry standard interconnect
- + Works with Industry standard MicroTCA and AdvancedTCA systems
- + Fast route to application code porting
- + Reduces risk and speeds time to market

The CommAgility AMC-V5Fe is a single width Advanced Mezzanine Card, mid or full-size depending on configuration. It is aimed at the latest applications requiring high performance FPGA processing and I/O, and also offers advanced capabilities in wireless and clock synchronisation should the application require this.

A Xilinx Virtex-5 LX110T FPGA provides the main processing. This configures and boots from FLASH on reset, using one of 4 selectable configuration images which are customer programmable and can be updated over Ethernet. The FPGA is fully customer configurable. The FPGA build may contain a MicroBlaze processor for basic board configuration and control, and a full example FPGA build and MicroBlaze Board Support Package is provided.

A 4x PCI Express interface is a key feature of the AMC-V5Fe, allowing low latency connection to a wide range of MicroTCA systems and CPUs. In addition there is a range of I/O provided including optical and serial interfaces with flexible clock synchronisation. A mezzanine site allows selected customers to add custom I/O or processing to the board if required.

A range of build options are available, and further customisation is possible in volume, to enable the best technical and commercial fit to a customer application to be achieved.



CommAgility Ltd
Loughborough, UK

www.commagility.com

Tel: +44 1509 228866
sales@commagility.com

Comm (Co)
Agility

Comm (Agility)

HARDWARE SPECIFICATIONS

FPGA: Xilinx Virtex-5™ FPGA. Standard configuration is LX110T-2, options include SX95T, LX155T. With:

- ♦ 2 independent banks of 128Mbytes x16 DDR2-600 SDRAM
- ♦ 128Mbytes of parallel FLASH
- ♦ 8Gbps 1x or 4x PCI Express connected to AMC ports 4-7, with Fclk support
- ♦ 2 Full-duplex Gigabit Ethernet ports
- ♦ 4x RocketIO™ to front panel 10Gbps CX4 connector, option to AMC ports 17-20

Optical Interface: 2 SFP sockets for optical CPRI RE/REC and OBSAI RP3-01 compliant antenna interface links, connected to FPGA RocketIO. Also usable for optical links such as sFPDP, FC, SRIO, GigE. Data rate up to 3.75Gbps per link.

Clock Synchronisation: Low-jitter OXCO based PLL, digitally controlled from the FPGA. Allows clock synchronisation and distribution from an external 30.72 MHz or 1PPS GPS clock via AMC backplane, front panel (option) or SFP SERDES. IEEE1588 is also possible.

Ethernet: Gigabit Ethernet infrastructure using Broadcom BCM5389™ switch:

- ♦ AMC.2 (1000BASE-BX) compliant connections to AMC Ports 0 & 1
- ♦ Full-duplex 1Gbps links

IPMI: ATmega128 IPMI controller:

- ♦ AMC.0 IPMB_L interface
- ♦ FRU EEPROM data
- ♦ Power and reset control
- ♦ Real-time health monitoring

Optional Mezzanine Site: Allows custom I/O or processing to be added:

- ♦ 54 Parallel and 4x RocketIO to FPGA
- ♦ 4x Gigabit Ethernet to switch
- ♦ Able to connect to front panel for I/O Usable by qualified OEM customers only.

Form Factor: Advanced Mezzanine Card

- ♦ AMC.0 Rev 2.0 compliant
- ♦ Mid-size or full-size depending on configuration; single-width
- ♦ For AdvancedTCA™ and MicroTCA™
- ♦ AMC.2 GigE and AMC.1 4x PCIe
- ♦ Hot swap support

CONFIGURATION AND DEBUG

- ♦ FPGA and MicroBlaze boot from FLASH.
- ♦ Choice of boot images, MMC controlled
- ♦ FLASH update utility allows new images to be downloaded over Ethernet.
- ♦ On-board debug LEDs for FPGA, power, Ethernet and SFP ports.
- ♦ Debug connector and breakout board for Xilinx JTAG and FPGA/MMC serial ports.

ENVIRONMENTAL/EMC/SAFETY

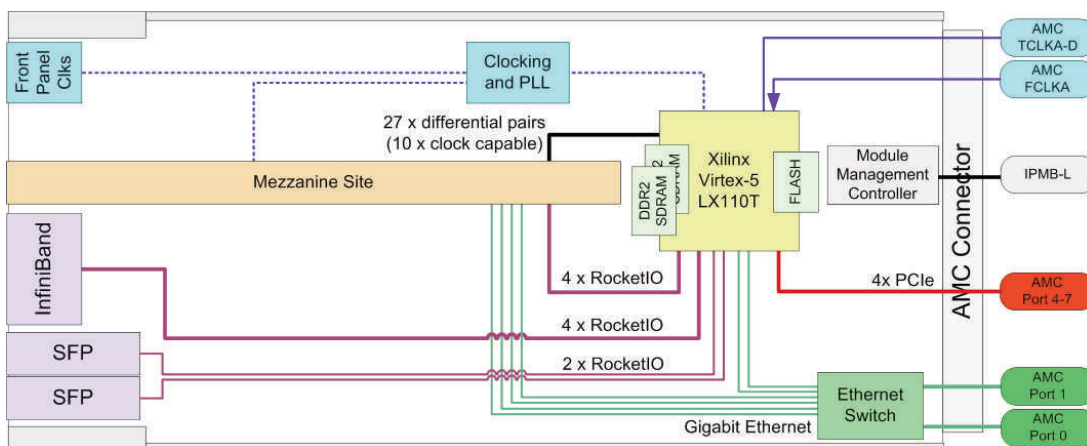
- ♦ Operating temperature: 0-40 °C ambient
- ♦ Power consumption: up to 28W max, dependent on SFPs used and FPGA load. Mezzanines will consume additional power
- ♦ Designed for NEBS and ETSI compliance when used in appropriate chassis
- ♦ 2004/108/EC and FCC EMC compliant
- ♦ 2002/95/EC RoHS, 2002/96/EC WEEE and 2006/95/EC Low Voltage Directive compliant

SOFTWARE SPECIFICATIONS

FPGA: to demonstrate configuration and functionality; Xilinx ISE and EDK project

MicroBlaze Board Support Library (BSL): support for board setup and interfaces, self test and FLASH update

MMC: full management suite based on PigeonPoint BMR software



OEM PARTNERSHIP SERVICES:

IN DEVELOPMENT support and training; hardware customisation; software and FPGA development.

IN MANUFACTURE leadtime reduction; extended warranty and repair; quick turn repairs and/or spares stocking. Licensing of designs considered for high volumes.

DURING LIFECYCLE obsolescence management; guaranteed lifecycle; Escrow.

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CommAgility Ltd
Loughborough, UK

www.commagility.com

Tel: +44 1509 228866
sales@commagility.com



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